

In the claims:

1. (Currently amended) A method of forming a layer of silicon on a surface of a workpiece comprising the steps of:
heating said workpiece on a substrate in a vacuum chamber;
depositing a layer of silicon on a surface of said workpiece ~~reacting at least two reactants to form said silicon;~~
in which said step of heating comprises supplying more than half of a total heating power to a lower surface of said workpiece, whereby said workpiece is maintained at a deposition temperature greater than a crystallization temperature of silicon during the depositing of the layer of silicon.
2. (Original) A method according to claim 1, in which said heating power is supplied by an upper set of lamps disposed above said workpiece and a lower set of lamps disposed below said substrate.
3. (Original) A method according to claim 2, in which approximately eighty percent of said heating power is supplied to said lower set of lamps.
4. (Original) A method according to claim 1, in which said substrate is maintained at a temperature of greater than 690°C.
5. (Original) A method according to claim 2, in which said substrate is maintained at a temperature of greater than 690°C.
6. (Original) A method according to claim 3, in which said substrate is maintained at a temperature of greater than 690°C.
7. (Original) A method according to claim 4, in which said substrate is maintained at a temperature of less than 710°C.

8. (Original) A method according to claim 5, in which said substrate is maintained at a temperature of less than 710°C.
9. (Original) A method according to claim 6, in which said substrate is maintained at a temperature of less than 710°C.
10. (Original) A method according to claim 1, in which said step of heating comprises supplying more than 75% of a total heating power to a lower surface of said workpiece.
11. (Original) A method according to claim 2, in which said step of heating comprises supplying more than 75% of a total heating power to a lower surface of said workpiece.
12. (Original) A method according to claim 3, in which said step of heating comprises supplying more than 75% of a total heating power to a lower surface of said workpiece.
13. (Original) A method according to claim 4, in which said step of heating comprises supplying more than 75% of a total heating power to a lower surface of said workpiece.
14. (Original) A method according to claim 5, in which said step of heating comprises supplying more than 75% of a total heating power to a lower surface of said workpiece.
15. (Original) A method according to claim 6, in which said step of heating comprises supplying more than 75% of a total heating power to a lower surface of said workpiece.
16. (Original) A method according to claim 7, in which said step of heating comprises supplying more than 75% of a total heating power to a lower surface of said workpiece.
17. (Original) A method according to claim 8, in which said step of heating comprises supplying more than 75% of a total heating power to a lower surface of said workpiece.

18. (Withdrawn) A field effect transistor comprising a body disposed between two electrodes, a gate insulator disposed over said body and below a gate, said gate being formed from silicon and having a first layer of polycrystalline silicon adjacent said gate insulator, with grains of silicon having a mean dimension less than 30nm.
19. (Withdrawn) A field effect transistor according to claim 18, in which said silicon gate has a layer of amorphous silicon on top of said layer of polycrystalline silicon, said layer of amorphous silicon and said first layer of polycrystalline silicon having been formed in the same process step.
20. (Withdrawn) A field effect transistor according to claim 18, in which said silicon gate has a second layer of polycrystalline silicon on top of said layer of polycrystalline silicon, said second layer of polycrystalline silicon having a mean grain size larger than 30nm and said second layer of polycrystalline silicon having been formed in the same process step as said first layer of polycrystalline silicon.